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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GERALD G. FAGERNESS, KERRY C. IMMING, BRIAN M. MCKEVETT, JAMES F. MIKOS, and TOLGA OZGUNER

Appeal 2009-006593
Application 10/625,954
Technology Center 2400

Before KENNETH W. HAIRSTON, JOHN C. MARTIN, and MARC S. HOFF, *Administrative Patent Judges*.

MARTIN, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-19, which are all of the pending claims.

We have jurisdiction under 35 U.S.C. § 6(b). We affirm-in-part.

A. Appellants' invention

Appellants' invention relates to determining a control block index for a data cell received by a network processor coupled to an ATM (asynchronous transfer mode[2]) network. Specification 3:10-12.

In an ATM network, data is transmitted using cells that include 48 bytes of information fields and 5 bytes of header fields (id. at 1:15-17). Routing occurs via virtual channel connections and virtual path connections, with virtual channel connections being addressed using a 16-bit virtual channel-identifier (VCI) and virtual path connections being addressed using a 12-bit virtual path identifier (VPI) (id. at6 1:15-21). The VCI and VPI for a data cell form part of the 5 bytes of header fields of the data cell (id. at 21-22).

Appellants' Figure 1 is reproduced below.

[2] Specification 1:13-14.

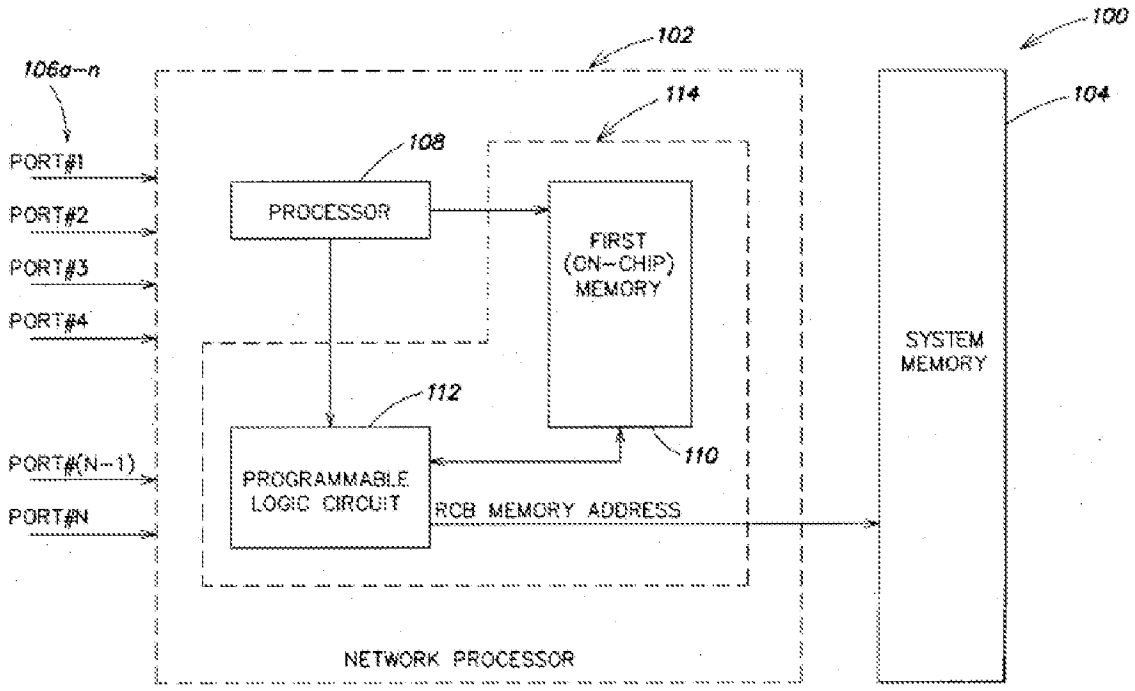

FIG. 1

Figure 1 is a block diagram of a network processor system 100 in accordance with the invention (*id.* at 4:28-31). Network processor circuit 102 has ports #1 to #N for receiving data cells transmitted over an ATM network (not shown) to which the network processor system 100 is coupled (*id.* at 5:5-9). A system memory 104 stores a plurality of RCBs (receive control blocks) including, for example, switching/control information for data cells received by the network processor circuit 102 (*id.* at 4:31-5:4). The RCB memory addresses, which as shown in Figure 1 are used for accessing system memory 104, are generated by "on-chip" hardware 114 that includes an "on-chip" memory 110 and a programmable logic circuit 112 (*id.* at 5:16-17).

Figure 2 is reproduced below.

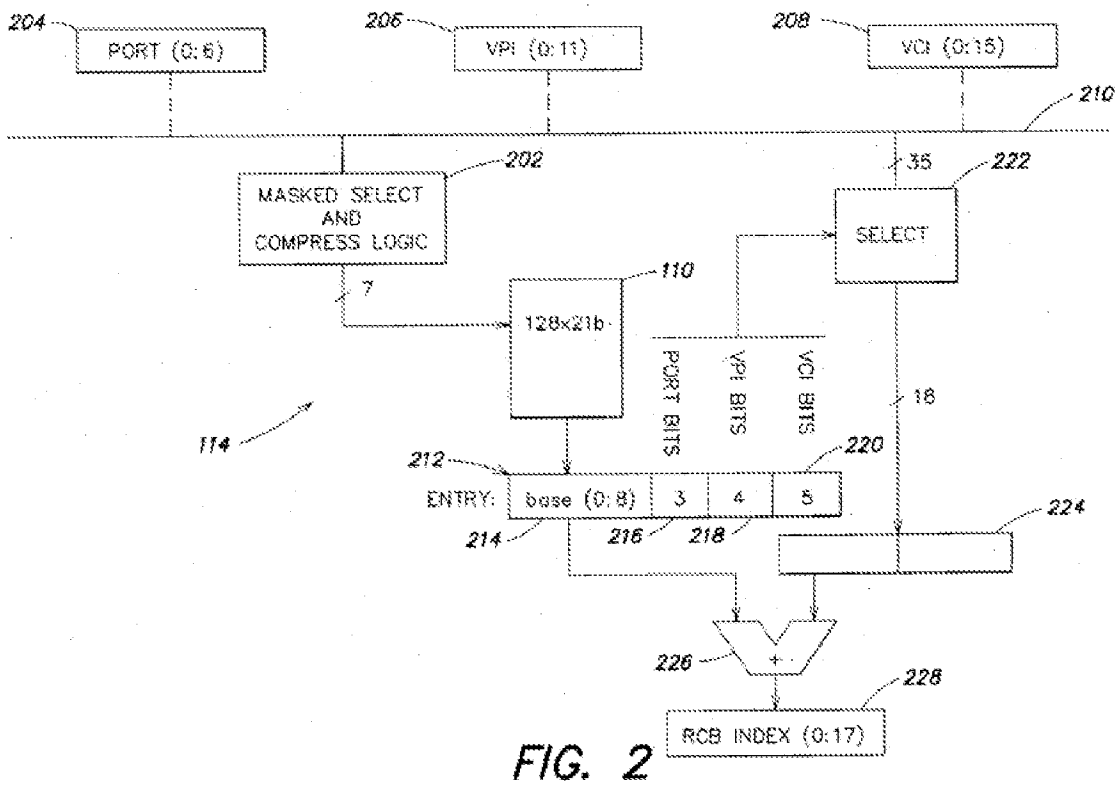

FIG. 2

Figure 2 shows an exemplary embodiment of on-chip hardware 114 (*id.* at 7:18-19). Circuitry (not shown) of the on-chip hardware 114 determines the port number 204, the VPI 206, and the VCI 208 associated with a received cell and provides one or more bits of the port number, VPI, and VCI to the masked select and compress logic 202 (*id.* at 7:29-33). The masked select and compress logic 202 generates an address based on the received bits (*id.* at 7:23-28). This address is also referred to as a "first index" (*e.g.*, *id.* at 3:30-4:5; claim 16).

On-chip memory 110, in response to receiving this address, outputs a corresponding entry 212 that includes, for example, (1) a first memory base

offset field 214, (2) a port number bits field 216, (3) a VPI bits field 218, and/or (4) a VCI bits field 220 (*id.* at 8:9-11, 28-31). The port number bits field 216 specifies the number of the bits (e.g., least significant bits) of port number 204 that will be selected by the selection circuit 222 (*id.* at 11:22-25). VPI bits field 218 and the VCI bits field 220 specify the number of bits (e.g., least significant bits) of VPI 206 and VCI 208 that will be selected by the selection circuit 222 (*id.* at 11:25-28). Thus, based on the values in bits fields 216, 218, and 220, selection circuit 222 selects the specified numbers of bits of the port number, VPI, and/or VCI and then outputs the selected eighteen bits to a register 224 (*id.* at 9:9-15). Of these bits (eighteen in number), adder 226 combines the nine most significant bits with the first memory base offset 214 to form an RCB index (*id.* at 14:32-15:3). This RCB index when added to a main system memory base offset forms the RCB memory address for accessing main system memory 104 (*id.* at 15:9-15).

B. The claims

The independent claims before us are claims 1, 11, 16, and 18. Claim 16 reads as follows:

> 16. A method for address mapping in a network processor, the method comprising:
>
> determining a port number of a port that receives a data cell;
>
> determining a virtual path identifier and a virtual channel identifier for the data cell;

creating a first index based on at least one of the port number, the virtual path identifier and the virtual channel identifier;

accessing one of a plurality of *entries stored in a first on-chip memory* using the first index;

creating a second index based on the accessed entry of the first on-chip memory; and

accessing an entry of a second memory based on the second index.

Claims App. (Br. 19-20) (emphasis added).[3]

C. The references

The Examiner's rejections are based on the following references:

Shtayer	US 5,414,701	May 9, 1995
Baentsch	US 6,272,504 B1	Aug. 7, 2001
Foglar	US 6,356,552 B1	Mar. 12, 2002

D. The rejections

Claims 16-19 stand rejected under 35 U.S.C. § 102(b) for anticipation by Shtayer. Final Action 4, para. 6.

Claims 1-3 and 5-15 stand rejected under 35 U.S.C. § 103(a) for obviousness over Shtayer in view of Foglar. *Id.* at 5, para. 9.

Claim 4 stands rejected under § 103(a) for obviousness over Shtayer in view of Foglar and Baentsch. *Id.* at 10, para. 10.

[3] Appeal Brief filed May 28, 2008.

THE § 102(b) REJECTION (CLAIMS 16-19)

Appellants argue that the rejection of claims 16-19 is erroneous because Shtayer fails to disclose accessing one of a plurality of entries stored in an "on-chip memory," as required by independent claims 16 and 18 (Br. 13-14). The term "on-chip memory" is defined in Appellants' Specification (at 5:14-15) as "refer[ring] to a memory that is on the same die or silicon as the network processor."

Shtayer discloses address compression in an asynchronous transfer mode (ATM) system. Shtayer, col. 1, ll. 8-11. Figure 2 of Shtayer is reproduced below.

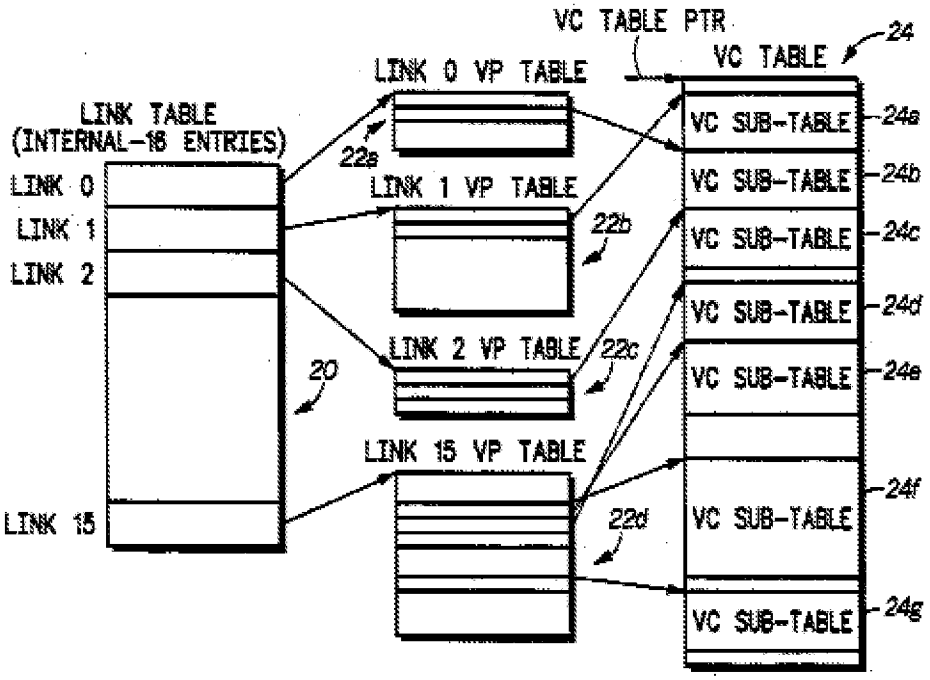

FIG.2

Figure 2 illustrates a link table 20 having sixteen entries (col. 4, ll. 42-43). Each entry points to a respective one of VP (virtual path) tables 22a-22d of a VP table (col. 4, ll. 52-53), whose entries point in turn to sub-tables 24a-24g of a VC (virtual channel table 24 (col. 5, ll. 13-16).

Figure 3 is reproduced below.

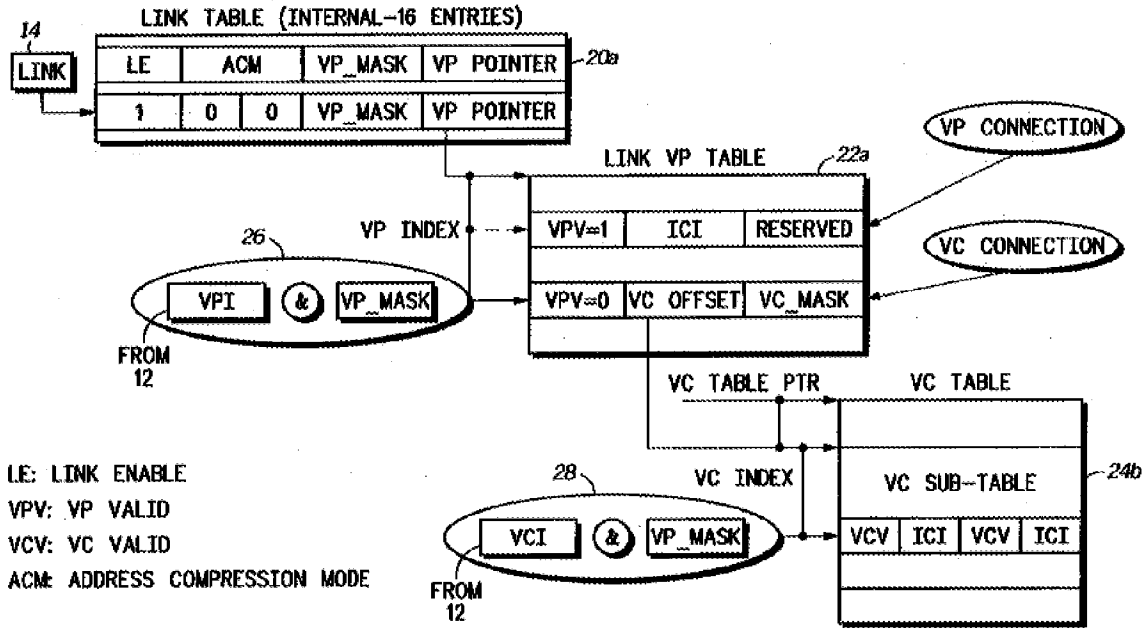

FIG.3

Figure 3 illustrates, in a block diagram, a more detailed view of a portion of the ATM address compression structure Figure 2 (col. 2, ll. 55-57).

In Figures 2 and 3 (and also in Figures 5 and 6), the link table is identified as "LINK TABLE (INTERNAL – 16 ENTRIES)." The "Internal" designation is not applied to the VP table or the VC table in any of the figures. Nor is the term "internal" used in Shtayer's specification. Although

not addressed by the Examiner or Appellants, we find that the term "external" is applied to a memory when discussing the function of an ICI (ingress connection/channel identifier[4]), an identifier stored in the VP and VC tables in Figure 3: "The ICI is the final result of the address compression process which is used to access connection-related parameters and flags in external memory to allow communication of an ATM data cell" (col. 5, ll. 7-10).

The Examiner reads that recited "plurality of entries" of independent claims 16 and 18 on Shtayer's link table (e.g., 20 in Figure 2) and finds that these entries are inherently stored in an on-chip memory, as required by these claims. As proof that the memory in which the link table is stored is inherently an on-chip memory, the Examiner relies on (1) the fact that the label "Internal" is applied to only the link tables in the figures and (2) the fact that of the three types of tables, the term "memory" is expressly applied to only the VP and VC tables. In the Examiner's words:

> Shtayer does not go into a lot of detail about this "Internal" property of the link table as it is not the novelty of his invention. However, it is evident to one of ordinary skill in the art that this is taken to mean the location of the table (i.e. "Internal" to the processing device). Shtayer emphasizes in numerous places that the Link VP and VC Tables are stored *in memory* (see lines 6-10 of column 2, for example). This language is used in the art to indicate a separate memory device (different than the small amount of memory typically available internal to the processing device itself (i.e. on-chip memory)). Applicant [sic: Shtayer] uses

[4] Shtayer, col. 4, ll. 66-67.

> this passage (and the numerous other similar passages) to distinguish the location of these tables from that of the link table (which is "Internal" to the processing device (and thus on-chip) as indicated in the figures themselves.)

(Answer 13.) Appellants counter that "no portion of Shtayer et al. connects these ["Internal"] notations with a location of the link table (i.e., on chip or off)" (Br. 13 (emphasis added)) and argue that an artisan would have understood that "Internal" refers to the fact that "there are 16 entries in the link table itself" (*id.*).

A reference anticipates under the principle of inherency if it *necessarily* functions in accordance with, or includes, the claimed limitations. *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986). We find that the meaning of "Internal" in the figures is ambiguous and therefore fails to support a finding of anticipation. *See In re Brink*, 419 F.2d 914, 917 (CCPA 1970) ("[I]f a reference is ambiguous and can be interpreted so that it may or may not constitute an anticipation of an appellant's claims, an anticipation rejection under 35 U.S.C. § 102 based upon the ambiguous reference is improper.").

We accordingly do not sustain the anticipation rejection of either of independent claims 16 and 18 or the rejection on that ground of either of dependent claims 17 and 19.

THE § 103(a) REJECTIONS (CLAIMS 1-15)

Claim 1 reads as follows.

> 1. A method for determining a control block index for a data cell received by a network processor coupled to an ATM

network comprising:

receiving a data cell at a port, the data cell having a virtual path identifier and a virtual channel identifier;

determining a port number for the port;

employing bits of at least one of the virtual path identifier, the virtual channel identifier and the port number to create a first address;

employing the first address to access a first memory and to obtain a first entry from the first memory, *the first entry specifying*:

a first base memory address;

a number of bits of the port number to use in the control block index;

a number of bits of the virtual path identifier to use in the control block index; and

a number of bits of the virtual channel identifier to use in the control block index; and

employing the first base memory address and the number of bits of the port number, virtual path identifier-and virtual channel identifier specified by the first entry to create the control block index for the data cell.

Claims App. (Br. 16) (emphasis added).

Appellants argue (Br. 11-12) that Shtayer and Foglar fail to disclose or suggest a memory entry that specifies a number of bits of a port number, as recited in claim 1 and also in independent claim 11. For such a teaching, the Examiner cites Foglar, which discloses an address conversion to be performed in an asynchronous transfer mode (ATM) switching station. Foglar, col. 4, ll. 54-59.

Foglar's Figure 1, on which the Examiner relies, is reproduced below.

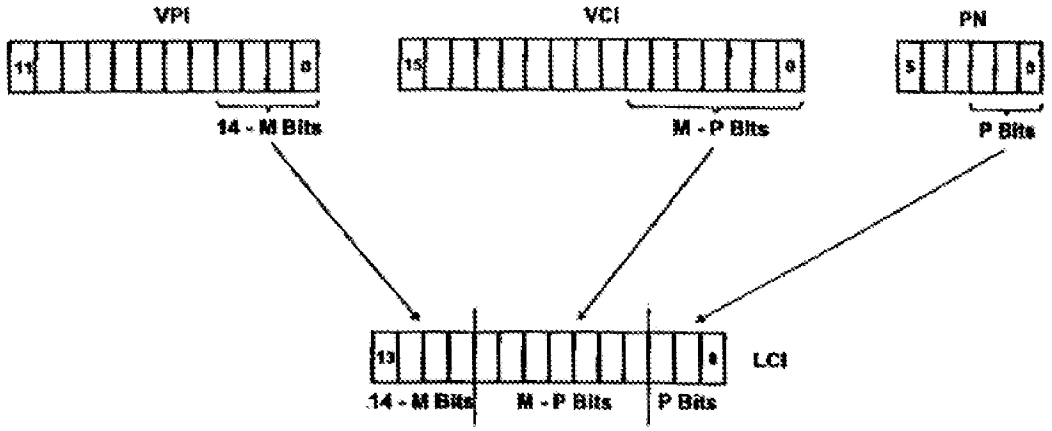

FIG 1

Figure 1 is a diagrammatic illustration of the forming of an address to be allocated to a set of values according to Foglar's invention (col. 4, ll. 35-37). A 14-bit LCI value, which is used as a reduced address, is formed of: (a) P bits of a 6-bit Physical Port Number PN; (b) 14-M bits of a 12-bit VPI (Virtual Path Identifier); and M-P bits of a 16-bit VCI (Virtual Channel Identifier) (col. 5, ll. 57-64). The value of PN "represents the number of the line or termination unit from which the applicable ATM cell has been received" (col. 5, ll. 64-67). Appellants apparently interpret Foglar's statement that "P. . . *represents* the number of lines or termination units (PHYs) with which the applicable ATM unit is connected" (col. 7, ll. 24-27)(emphasis added) as defining P to be equal to the total number of connected ports (Br. 12). This interpretation overlooks Foglar's more

specific explanation that "[i]n the example in question, 2^P is equal to the number of lines or termination units connected to the applicable ATM unit" (col. 7, ll. 27-29). Thus, as explained by the Examiner, "if the value of P is 3, the port number parameter is 3 bits long (*P bits long*) and will support $8=2^p$ ports (or lines or termination units)" (Answer 12). It is therefore clear that P in Figure 1 defines a number of bits of the number PN of the port that is receiving the corresponding ATM cell. We therefore agree with the Examiner that "[t]he value of P is clearly the number of *port bits* used in the creation of the LCI" (Answer 12) and disagree with Appellants' assertion that "Foglar's discussion of P bits does not disclose 'a number of bits of a port number as recited in independent claims 1 and 11" (Reply Br. 4).

The rejection of claims 1 and 11 is sustained, as are the rejections of dependent claims 2-10 and 12-15, which are not separately argued. *In re Nielson*, 816 F.2d 1567, 1572 (Fed. Cir. 1987).

DECISION

The rejection of claims 16-19 under 35 U.S.C. § 102(b) for anticipation by Shtayer is not sustained.

The rejection of claims 1-3 and 5-15 under 35 U.S.C. § 103(a) for obviousness over Shtayer in view of Foglar is sustained, as is the rejection of claim 4 under § 103(a) for obviousness over Shtayer in view of Foglar and Baentsch.

The Examiner's decision that claims 1-19 are unpatentable is accordingly affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1). *See* 37 C.F.R. § 1.136(a)(1)(v) (2010).

AFFIRMED-IN-PART

gvw

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